

IN THE  
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Frederick A. Perner et al.

Confirmation No.:

Application No.:

Examiner:

Filing Date: herewith

Group Art Unit:

Title: SYSTEM AND METHOD FOR READING A MEMORY CELL

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or  
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:  
( ) Statement under 37 CFR 1.97(e), or  
( ) a \$180.00 fee under 37 CFR 1.17(p), or  
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:  
( ) Statement under 37 CFR 1.97(e)(1) or (2), and  
( ) a \$180.00 fee set forth in 37 CFR 1.17(p).  
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **ET891040803US**

Respectfully submitted,

Date of Deposit July 7, 2003

Frederick A. Perner et al.

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By

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Reg. No. 39, 766

Date: July 7, 2003

FORM PTO-1449		ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		200208959-1		
(Use several sheets if necessary)		APPLICANT Frederick A. Perner		
		FILING DATE	GROUP	
		herewith		

## REFERENCE DESIGNATION                    U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
1A	6,169,686B1	Jan. 2, 2001	Brug et al.	
1B	6,259,644B1	Jul. 10, 2001	Tran et al.	
1C	6,567,297 B2	May 20, 2003	R. Jacob Baker	
1D	2002/0101758	Aug. 1, 2002	R. Jacob Baker	
1E	2003/0039162	Feb. 27, 2003	R. Jacob Baker	
1F				
1G				
1H				
1I				
1J				
1K				

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
1L					
1M					
1N					
1O					
1P					

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

1Q	"Nonvolatile RAM based on Magnetic Tunnel Junction Elements" by M. Durlam et al. 2000 IEEE International Solid-State Circuits Conference 07803-5853-8/00, Motorola Labs, Physical Sciences Research Labs, Tempe, AZ, Section TA 7.3
1R	"A 10ns Read and Write Non-volatile Memory Array Using a Magnetic Tunnel Junction and FET Switch in each Cell" by Roy Scheuerlein et al. 2000 IEEE International Solid-State Circuits Conference 07803-5853-8/00, IBM Research Almaden Research Center, San Jose, CA, Section TA 7.2
1S	"Offset Compensating Bit-Line Sensing Scheme for High Density DRAM's" by Yohi Watanabe et al., IEE Jurnal of Solid-State Circuits, Vol. 29, No. 1, January 1994.